

REPETITIVE CURRENT CONTROL TOPOLOGY FOR GRID-CONNECTED BOOST-HALF-BRIDGE PHOTOVOLTAIC MICRO INVERTER

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ABSTRACT

This paper presents a novel Repetitive Current control topology for grid-connected boost half- bridge photovoltaic (PV) micro inverter system. To reduce the cost, easy control, improving efficiency, and high reliability, boost-half-bridge dc–dc converter using minimal devices is introduced to interface the low-voltage PV module. A full-bridge inverter with pulse width-modulator is cascaded and injects synchronized sinusoidal current to the grid. In addition, a plug-in repetitive current controller based on a fourth-order linear phase IIR filter is proposed to regulate the grid current. Through this approach we obtained high power factor and very low total harmonic distortions under both heavy load and light load conditions. Dynamic stiffness is obtained when load or solar irradiance is changing rapidly. In addition, the dynamic behavior of the boost-half-bridge dc–dc converter is analyzed; a customized maximum power point tracking (MPPT) method, which generates a ramp-changed PV voltage reference, is developed accordingly. Variable step size is embrace such that fast tracking speed and high MPPT efficiency are both obtained. Simulation results are provided to verify the validity and performance of the circuit operations, current control, and MPPT algorithm.

KEYWORDS: Repetitive Current Control Topology, MPPT Algorithm, Fourth-Order Linear Phase

INTRODUCTION

The future trend for single-phase grid-connected photovoltaic (PV) power systems for reduction of mismatches of among PV modules, optimal design of individual PV-module, improving the maximum power point tracking the concept of micro inverter (also known as module integrated converter/inverter) is become more popular. In general, a PV micro inverter system is frequently supplied by a low-voltage solar panel, which needs a high-voltage step-up ratio to produce desired output ac voltage [1]–[3]. So, a dc–dc converter cascaded by an inverter is the most popular topology, in which a HF transformer is often implemented within the dc–dc conversion stage [4]–[10]. For implementation of pulse width modulation (PWM) techniques to the PV micro inverter system, two major categories are attracting most of the attentions. In the first, PWM control is applied to both the dc–dc converter and the inverter [4]–[6]. However, a constant voltage dc link decouples the power flow in the two stages such that the dc input is not affected by the double-line-frequency power ripple become visible at the ac side. In the second configuration utilizes a quasi-sinusoidal PWM method to control the dc–dc converter in order to generate a rectified sinusoidal current (or voltage) at the inverter dc link. Based on a line-frequency-commutated inverter unfurls the dc-link current (or voltage) to attain the sinusoidal form synchronized with the grid [7]–[10]. Even though the latter has the advantage of higher conversion efficiency because of the elimination of HF switching losses at the inverter, the double line- frequency power ripple must be all absorbed by the dc input capacitor, formulating the MPPT efficiency (defined as the ratio of the energy drawn by the PV inverter within a certain measuring

period at the steady state to the theoretical available energy from the PV module) compromised unless a very large capacitance is used. Like wise, the dc–dc conversion stage requires more challenging control techniques to meet the grid current regulation requirement. Hence, in terms of the MPPT performance and output current quality, the first category of PV micro inverter is more appropriate and will be espoused in this paper. A boost dual-half-bridge dc–dc converter for bidirectional power conversion applications was first proposed in [11] and then further examined in [12]–[14]. It integrates the boost converter and the dual-half-bridge converter together by using minimal number of devices. High efficiency is attainable when the zero-voltage switching (ZVS) technique is adopted. By put back of the secondary half bridge through a diode voltage doublers, a new boost-half-bridge converter can be derived for unidirectional power conversions [15]. In this paper, the boost half-bridge converter is included as the dc–dc conversion stage for the grid-connected PV micro inverter system. Assistance from its circuit simplicity, ease of control, and minimal semiconductor devices, the hopeful features such as low cost, high efficiency, and high reliability are obtained.

A full-bridge PWM inverter through an output *LCL* filter is incorporated to inject synchronized sinusoidal current to the grid. In general, its performance is estimated by the output current total harmonic distortions (THDs), power factor, and dynamic response. Repetitive control (RC) is known as an effective solution for removing of periodic harmonic errors and has been previously investigated and validated in the uninterruptible power system (UPS) systems [16]–[24], active power filters [25]–[28], boost-based PFC circuits [29], and grid connected inverters/PWM rectifiers [30]–[32]. In [24], a fourth order linear-phase IIR filter has been manufactured for the RC based UPS systems. This IIR filter is executed to obtain very high system open-loop gains at a large number of harmonic frequencies such that the harmonic rejection capability is greatly enhanced. In this paper, a plug-in repetitive current controller is proposed. It is unruffled of a proportional part and an RC part, to which the IIR filter in [24] is accommodated. The proposed current controller demonstrates the following superior features:

- High power factor is obtained;
- Current harmonic distortions (up to the 13th-order) caused by the grid voltage no ideality are minimized;
- Outstanding current regulation is guaranteed within a wide range of load conditions;
- Fast dynamic response is achieved during the transients of load or solar irradiance change.

MPPT is carry out by the boost-half-bridge dc–dc converter. Numerous MPPT techniques have been studied and validated, for example, perturb and observe (P&O) method [35]–[38], incremental conductance method [39], ripple correlation method [40], reduced current sensor method [41], etc. Different techniques have exposed different tradeoffs among the steady-state MPPT efficiency, the transient tracking speed, and the control complexity [42], [43]. Another grave concern for MPPT implementation is the dynamics of the particular converter adopted.

In [37], an optimal P&O method has been developed to bound the negative effect of the converter dynamic responses on the MPPT efficiency. In [38], a closed-loop control technique has been proposed to reduce the PV voltage oscillation. However, the converter dynamic behavior related with the MPPT operation can also influence the converter efficiency and functioning, which has been rarely discussed previously. For example, the MPPT methods with step-changed perturbations on the PV voltage (or current) or the converter duty cycle periodically may sometimes Leads to problems such as inrush current, *LC* oscillation, magnetic saturation, etc.

These undesirable transient responses can cause the higher power losses or even circuit malfunctioning, and of course, they are different from case to case. In this paper, the dynamics of the boost-half-bridge converter is vigilantly studied for guiding the MPPT design. A customized MPPT creating a ramp-changed PV voltage is then developed for practice. In addition, for the reason of fast tracking and high MPPT efficiency, the power-voltage (P - V) curve of the PV module is divided into three different operation zones, where the MPPT step size is varied accordingly.

BOOST-HALF-BRIDGE PV MICRO INVERTER

The boost-half-bridge micro inverter topology for grid connected PV systems is shown in Figure 1. It is collected of two decoupled power processing stages. In the front-end dc-dc converter, a conventional boost converter is changed by splitting the output dc capacitor into two separate ones. C_{in} and L_{in} denote the input capacitor and boost inductor, respectively. The center taps of the two MOSFETs ($S1$ and $S2$) and the two output capacitors ($C1$ and $C2$) are linked to the primary terminals of the transformer Tr , just like a half bridge type. The transformer leakage inductance reflected to the primary is represented by L_s and the transformer turns ratio is $1:n$. A voltage doubler unruffled of two diodes ($D1$ and $D2$) and two capacitors ($C3$ and $C4$) is incorporated to rectify the transformer secondary voltage to the inverter dc link. A full-bridge inverter unruffled of four MOSFETs ($S3$ - $S6$) using synchronized PWM control behaves as the dc-ac conversion stage. Sinusoidal current with a unity power factor is supplied to the grid through a third-order LCL filter ($Lo1$, $Lo2$, and Co). Other symbolic representations are defined as follows. The duty cycle of $S1$ is denoted by $d1$.

The switching period of the boost half-bridge converter is T_{sw1} . The PV current and voltage are represented by i_{PV} and v_{PV} , respectively. The voltages across $C1$, $C2$, $C3$, and $C4$ are indicated by v_{c1} , v_{c2} , v_{c3} , and v_{c4} , respectively. The transformer primary voltage, secondary voltage, and primary current are indicated as v_{r1} , v_{r2} , and i_{r1} , respectively. The low-voltage side (LVS) dc-link voltage is v_{dc1} and the high voltage side (HVS) dc-link voltage is v_{dc2} . The switching period of the full bridge inverter is T_{sw2} . The output ac currents at the inverter side and the grid side are indicated by i_{inv} and i_g , respectively. The grid voltage is v_g .

The boost-half-bridge converter is controlled by $S1$ and $S2$ with corresponding duty cycles. Neglect all the switching dead bands for easy purpose. The idealized transformer working performance waveforms are illustrated in Figure 2. When $S1$ is ON and $S2$ is OFF, v_{r1} equals to v_{c1} . When $S1$ is OFF and $S2$ is ON, v_{r1} equals to $-v_{c2}$. At the steady state, the transformer volt-second is being automatically balanced. And also represented as the primary volt-second $A1$ (positive section) and $A2$ (negative section) are equal, so are the secondary volt-sec $A3$ (positive section) and $A4$ (negative section). Normally, $D1$ and $D2$ are ON and OFF in a related manner as $S1$ and $S2$, but with a phase delay t_{pd} due to the transformer leakage inductance. Ideally, the transformer current waveform is evaluated by the relationships of $v_{c1} - -v_{c4}$, the leakage inductance L_s , the phase delay t_{pd} , and $S1$'s turn-ON time $d1T_{sw1}$ [12].

In order to obtain an optimal efficiency of the boost-half-bridge converter, the ZVS techniques can be considered for practical implementation, as guided by [12]. It is importance noting that engineering tradeoffs must be made among the reduced switching losses and increased conduction losses when soft switching is implemented. For simplicity, hard switching is implemented and the transformer leakage inductance is regarded as small sufficient in this paper. Therefore, (1) and (2) can be obtained as follows:

$$v_{c1} = \frac{(1-d_1)}{d_1} v_{PV} \quad v_{c2} = v_{PV} \quad v_{dc1} = \frac{v_{PV}}{d_1} \quad (1)$$

$$v_{c3} = \frac{n(1-d_1)}{d_1} v_{PV} \quad v_{c4} = n v_{PV} \quad v_{dc2} = \frac{n v_{PV}}{d_1} \quad (2)$$

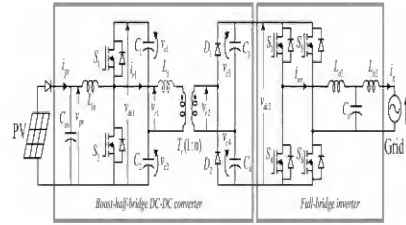


Figure 1: Topology of the Boost-Half-Bridge PV Micro Inverter

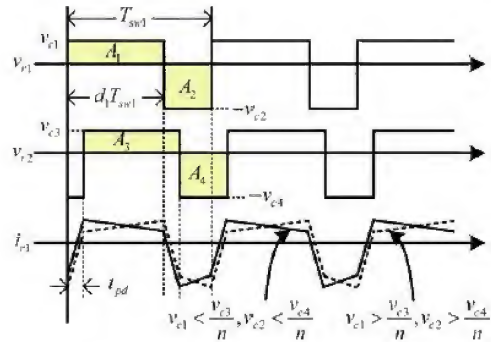


Figure 2: Idealized Transformer Voltage and Current

When observing from the full-bridge inverter, the boost-half bridge converter just operates similarly as a conventional boost converter, but with the extra benefits of the galvanic isolation as well as the high step-up ratio. The simple circuit topology with minimal use of semiconductor devices exhibits a low total cost and good reliability.

SYSTEM CONTROL DESCRIPTION

An all-digital approach is implemented for the control of the boost half- bridge PV micro inverter system, as shown in Figure 3. The PV voltage v_{PV} and current i_{PV} are both measured for calculation of the instantaneous PV power P_{pv} , the PV power variation ΔPPV , and the PV voltage variation Δv_{PV} . The MPPT function block evaluates a reference v^*_{PV} for the inner loop of the PV voltage regulation, which is executed by the dc–dc converter. At the inverter side, the grid voltage v_g is measured to perfect the instantaneous sinusoidal angle θ_g , which is commonly known as the phase lock loop (PLL). The inverter output current i_{inv} is pre filtered by a first-order low-pass filter on the sensing circuitry to remove the HF noises.

The filter output i_{inv} is then fed back to the plug-in repetitive controller for the inner loop control. Either v_{dc1} or v_{dc2} can be measured for the dc-link voltage regulation as the outer loop. In practice, the LVS dc-link voltage v_{dc1} is regulated for reducing the cost. The grid current and the LVS dc link voltage references are denoted by i^*_{inv} and v^*_{dc1} , respectively.

In turn to achieve fast dynamic responses of the grid current and also the dc-link voltage, a current reference feed forward is added in accordingly to the input PV power PPV . The magnitude of the current feed forward is expressed as follows:

$$|i_{inv}|_{ff} = \frac{2P_{PV}}{|v_g|} \quad (3)$$

Where $|v_g|$ is the magnitude of the grid voltage and can be evaluated by

$$|v_g| = \frac{1}{2} \int_0^\pi v_g d\theta_g. \quad (4)$$

PLUG-IN REPETITIVE CURRENT CONTROLLER

Up to now, using an *LCL* filter in a grid-connected inverter system has been predictable as an effective solution to reduce current harmonics around the switching frequency, increase the system dynamic response, and decrease the total size and cost [44]. Typically, an un damped *LCL* filter shows a sharp *LC* resonance peak, which indicates a potential stability issue for the current regulator construction. Therefore, either passive damping or active damping techniques can be espoused to attenuate the resonance peak below 0 dB [45], [46]. Alternatively, a current regulator without introducing any damping method can also be stabilized, as long as the *LCL* parameters and the current sensor location are correctly selected [47]. In this paper, the *LCL* parameters are selected by as per the guidelines provided in [44] and [47]. The current sensor is placed at the inverter side as a substitute of the grid side. Resultantly, no damping techniques are wanted such that the current control is more simplified. Table 1 summarizes the key parameters of the full-bridge inverter.

- **Plant Transfer Function**

The control-output-to-inverter-current transfer function in the continuous time domain can be validated as (5), where $r1$ and $r2$ represent the equivalent series resistance of $Lo1$ and $Lo2$, accordingly. Based on the power loss estimation of the inductors, $r1 = 1.4 \Omega$ and $r2 = 1.0 \Omega$

$$G_{LCL}(s) = \frac{L_{o2}C_o s^2 + r_2 C_o s + 1}{L_{o1}L_{o2}C_o s^3 + (r_1 L_{o2} + r_3 L_{o1})C_o s^2 + (r_1 r_3 C_o + L_{o1} + L_{o2})s + r_1 + r_3} e^{-sT_d}. \quad (5)$$

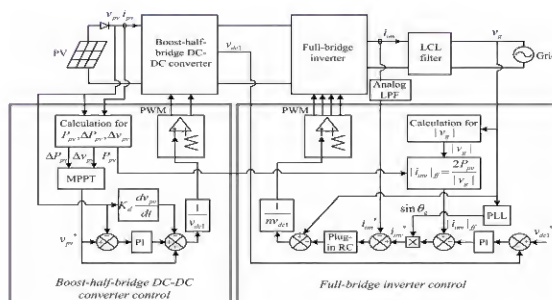


Figure 3: Architecture of the Proposed PV Micro Inverter System Control

TABLE I
FULL-BRIDGE INVERTER PARAMETERS

HVS DC link voltage	370 V
Switching frequency	10.8 kHz
Sampling frequency	10.8 kHz
Rated output power	210 W
Grid voltage	180
Grid line frequency	60 Hz
Filter inductor (L_{o1}, L_{o2})	8.5 mH
Filter capacitor (C_o)	330 nF

From (5), the LC resonance frequency is

$$\omega_r = \sqrt{\frac{r_1 r_2 C_o + L_{o1} + L_{o2}}{L_{o1} L_{o2} C_o}}. \quad (6)$$

So as to reduce the switching noises in the sensed inverter current, an analog low-pass filter (7) is placed on the current feedback path

$$F_{LPF}(s) = \frac{\omega_{fc}}{s + \omega_{fc}}. \quad (7)$$

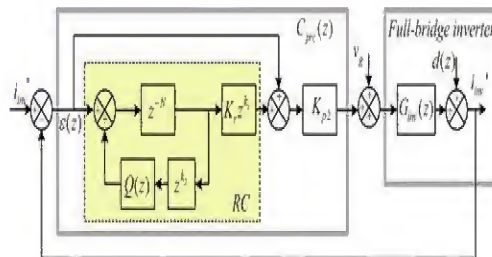


Figure 4: Block Diagram of the Proposed Plug-in Repetitive Controller

The cutoff frequency is selected as $\omega_{fc} = 4 \times 10^4$ rad/s. So, by using the zero-order hold discretization scheme, the total plant combining (5) and (7) can be discretized as (8).

$$G_{inv}(z) = \frac{0.00265z^{-2} + 0.00548z^{-3} + 0.00474z^{-4} + 0.00559z^{-5} + 0.000254z^{-6}}{1 + 0.5468z^{-1} - 0.5653z^{-2} - 0.9606z^{-3} + 0.024z^{-4}} \quad (8)$$

Plug-in RC Scheme

The plug-in digital repetitive controller is designed, as shown in Figure 4. The conventional proportional controller with a gain of K_{p2} is incorporated to fast dynamics. The RC is then plugged in and functioning in parallel with the proportional controller. $e(z)$ and $d(z)$ represent the tracking error and the repetitive disturbances, respectively. The modified internal model [33], which is represented by the positive feedback loop inside the RC, plays the mainly critical role in the proposed current regulator. z^{-N} is the time delay unit, where N denotes the number of samples in one fundamental period.

In an ideal RC, a unity gain is along the positive feedback path such that all the repetitive errors based on the fundamental period are totally eliminated when the system reaches equilibrium. Then again, in order to attain a sufficient stability margin, a zero-phase low-pass filter is often included rather than the unity gain. This can be understudied by cascading a linear-phase low pass filter $Q(z)$ and a non causal phase lead compensator zk^2 . zk^1 is another non causal phase lead unit, which compensates the phase lag of $G_{inv}(z)$, particularly, at HF's [21]. Here k_1 and k_2 both stand for the number of sampling periods. K_r is the constant gain unit that determines the weight of the RC in the whole control system. From Figure 4, the transfer function of the entire plug-in RC current regulator can be described as follows:

$$C_{pre}(z) = \frac{K_r K_{p2} z^{-N} z^{k_1}}{1 - Q(z) z^{k_2} z^{-N}} + K_{p2}. \quad (9)$$

Analysis and Design of the Plug-in RC

The selection of K_{p2} follows accurately the same rules as the conventional proportional controller design. Basically, it need a tradeoff between the obtainable stability margin and the current regulation performance. In this paper, $K_{p2} = 50$. From Figure 4, the tracking error $\varepsilon(z)$ can be derived as follows:

$$\begin{aligned} \varepsilon(z) = \varepsilon(z)z^{-N} & \left[Q(z)z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{inv}(z)}{1 + K_{p2} G_{inv}(z)} \right] \\ & + \left[\frac{1 - Q(z)z^{k_2} z^{-N}}{1 + K_{p2} G_{inv}(z)} \right] [i_{inv}^*(z) - d(z)] \quad (10) \end{aligned}$$

It is perceptible that a larger K_{p2} will result in a smaller tracking error throughout the transient because the second summation term on the right side of (10) is reduced. This accurately explains the function of the proportional control part

Let

$$\begin{aligned} |H(z)|_{z=e^{j\omega T_{sw2}}} &= \left| Q(z)z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{inv}(z)}{1 + K_{p2} G_{inv}(z)} \right|, \\ \omega &\in \left[0, \frac{\pi}{T_{sw2}} \right] \end{aligned}$$

In which T_{sw2} is also the sampling period A enough condition to meet the stability requirement is

$$|H(e^{j\omega T_{sw2}})| < 1. \quad (11)$$

At the fundamental and harmonic frequencies, z^{-N} is simply equal to unity. Therefore, the steady-state error can be derived from (10) as follows:

$$|\varepsilon(z)| = |i_{inv}^*(z) - d(z)| \left| \frac{1 - Q(z)z^{k_2}}{[1 + K_{p2} G_{inv}(z)][1 - H(z)]} \right|. \quad (12)$$

From (11) and (12), the common design criteria of $Q(z)$ for obtaining a good stability as well as a small steady-state error can be recapitulated as:

- $Q(z)$ must have sufficient attenuation at HFs;
- $Q(z)$ must be close to unity in a frequency range, which covers a large number of harmonics; and
- $Q(z)z^{k_2}$ must have a zero phase when $Q(z)$ is close to unity.

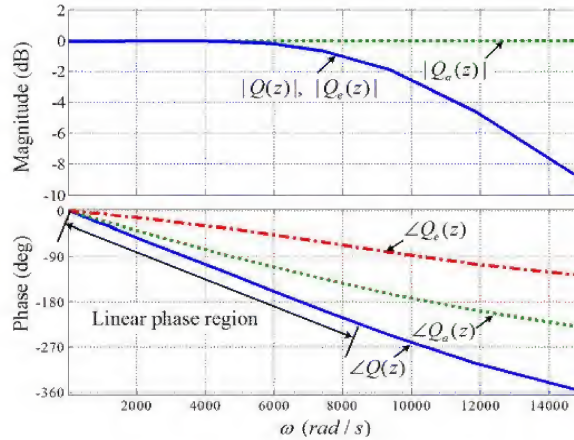


Figure 5: Bode Plots of $Q_e(z)$, $Q_a(z)$, and $Q(z)$

In [24], a fourth-order linear-phase IIR filter has been manufactured for the repetitive voltage controller for UPS systems. Compared with the conventional linear-phase finite impulse response filters used for RC, the linear-phase IIR filter demonstrates a flat gain in the pass band and a large amount faster roll off in the transition band, when the filter order is given [24], [34]. So, it is a good candidate for the repetitive current controller in this paper as well. In practice, $Q(z)$ is synthesized by cascading a second-order elliptic filter $Q_e(z)$ and a second-order all-pass phase equalizer $Q_a(z)$. $Q(z)$, $Q_e(z)$, and $Q_a(z)$ are obtained from MATLAB and expressed by (13)–(15)

$$Q(z) = Q_e(z)Q_a(z) \quad (13)$$

$$Q_e(z) = \frac{0.1385 + 0.2564z^{-1} + 0.1385z^{-2}}{1 - 0.7599z^{-1} + 0.2971z^{-2}} \quad (14)$$

$$Q_a(z) = \frac{0.1019 - 0.6151z^{-1} + z^{-2}}{1 - 0.6151z^{-1} + 0.1019z^{-2}} \quad (15)$$

The bode plots of $Q_e(z)$, $Q_a(z)$ and $Q(z)$ are shown in Figure 5. The linear-phase region of $Q(z)$ is from 0 to 1403 Hz (8816 rad/s). In order to balance the phase delay of $Q(z)$ to zero in this region, $k_2 = 5$ is selected. The maximum pass band gain and the cutoff frequency of $Q(z)$ are 0.9975 and 1670 Hz, correspondingly.

BOOST-HALF-BRIDGE CONVERTER CONTROL

Table 1 review the key parameters of the boost-half bridge dc–dc converter. As aforementioned, the PV voltage is regulated instantly to the command generated by the MPPT function block. The continuous-time control block diagram is shown in Figure 6. High bandwidth proportional-integral control is espoused to track the voltage reference ϖ^*_{PV} and to reduce the double-line-frequency disturbance from the LVS dc link. The capacitor voltage differential feedback is presented for active damping of the input LC resonance [48]. Normally, the MPPT function block in a PV converter/inverter system periodically changes the tracking reference of the PV voltage, or the PV current, or the modulation index, or the converter duty cycles. In the majority cases, these periodic perturbations yield step change dynamic responses in power converters. If the converter dynamics are overlooked in the MPPT control, undesirable transient responses such as LC oscillation, inrush Current, and magnetic saturation may take place. Accordingly, the conversion efficiency can be deteriorated or even malfunction of the converter may occur.

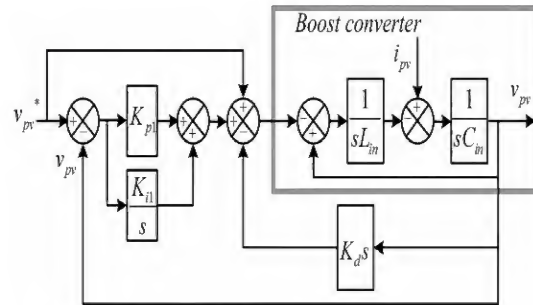


Figure 6: Block Diagram of the PV Voltage Regulator

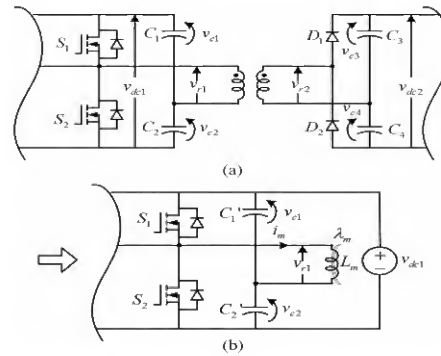
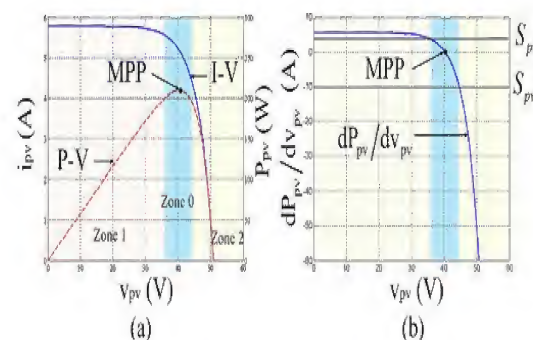


Figure 7: a) Half-Bridge Converter Part b) Equivalent Circuit Seen from the LVS Dc Link of (a)

Equations (1) and (2) indicate that v_{c1} – v_{c4} are varying dynamically in accordance with $d1$. It is worth noting that the charge and discharge of $C1$ – $C4$ caused by the odd voltage distribution on the upper capacitors ($C1$ and $C3$) and the lower capacitors ($C2$ and $C4$) can only be conducted through the transformer magnetizing inductor. Which result, at any time, the charge and discharge rate of $C1$ – $C4$ must be bounded such that the transformer flux is not saturated. Instinctively, this can be done by either introducing the transformer flux as a state variable into the inner PV voltage regulator or designing the outer MPPT block adaptively. For the sake of control simplicity and low cost, developing a customized MPPT method by sympathetically taking care of the boost-half-bridge converter dynamics would be more attractive.


 Figure 8: a) I-V, P-V Curves b) PV Operation Zone Division Based on dP_{pv}/dv_{pv}

Dynamics of the Boost-Half-Bridge Converter

As before discussed, the boost-half-bridge converter can be considered as the integration of two subcircuit topologies: 1) the boost converter and 2) the half-bridge converter. The PV voltage regulator depicted in Figure 6 has ensured that both the steady state and the dynamic response of the boost converter part are fully care of. Hence, the following analysis will be only concentrated on the dynamics of the half-bridge converter part.

The main role of the half-bridge converter here is to transfer energy from the LVS dc link to the HVS dc link by means of the transformer. But besides that, it also allocates the amount of stored charges on the upper dc-link capacitors ($C1$ and $C3$) and the lower dc-link capacitors ($C2$ and $C4$). Neglecting the effect of the transformer leakage inductance and power losses at this time, Figure 7 depicts the extracted half bridge converter part and its comparable circuit seen from the LVS dc link. As v_{dc1} is regulated to a constant dc, the LVS dc link in Figure 7(b) is simply connected to a constant voltage source for approximation. $C3$ and $C4$ are both reflected to the transformer primary and combined with $C1$ and $C2$. C_{-1} and C_{-2} stand for the equivalent dc-link capacitors, where $C_{-1} = C1 + n2C3$ and $C_{-2} = C2 + n2C4$. L_m , i_m , and λ_m indicate the transformer primary magnetizing inductor, dc current, and dc flux linkage,

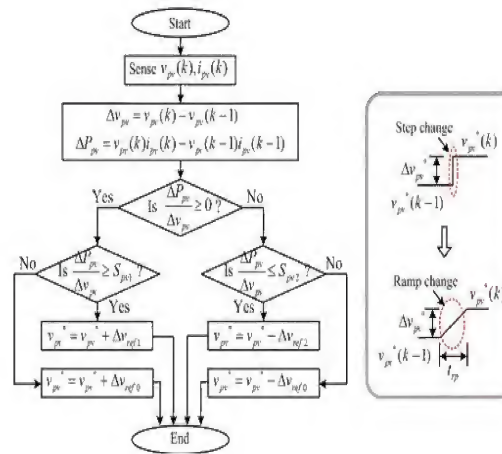


Figure 9: Flow Chart of the Variable Step-Size MPPT

correspondingly. At the steady state, both i_m and λ_m are zero. But once the converter duty cycle d_1 is perturbed, i_m and λ_m will increase or decrease such that the electric charges can be transferred from C_{-1} to C_{-2} or vice versa. According to the

Faraday's law, one has

$$v_{c1}(t)d_1(t) - v_{c2}(t)(1 - d_1(t)) = \frac{d\lambda_m(t)}{dt}. \quad (16)$$

Define the duty cycle change rate $d_{-1}(t) = d(d_1(t))/dt$. Take derivative on both sides of (16), then

$$v_{dc1}d_1'(t) - \frac{dv_{c2}(t)}{dt} = \frac{d^2\lambda_m(t)}{dt}. \quad (17)$$

Furthermore, the capacitor charge and discharge equation can be expressed as follows:

$$(C_1' + C_2')\frac{dv_{c2}(t)}{dt} = i_m(t) = \frac{\lambda_m(t)}{L_m}. \quad (18)$$

Plug (18) into (17), then

$$\frac{d^2\lambda_m(t)}{dt} + \frac{\lambda_m(t)}{L_m(C_1' + C_2')} - v_{dc1}d_1'(t) = 0. \quad (19)$$

Equation (19) illustrates the dynamics of a typical second-order system, where $d_{-1}(t)$ is the excitation and $\lambda_m(t)$

is the response. If d_1 is constant initially (at the steady state) and then perturbed by the MPPT operation, λ_m will start to oscillate with a frequency of $1/(2\pi\sqrt{L_m(C'_1 + C'_2)})$. Defining the magnitude of λ_m as $|\lambda_m|$ and assuming $d_{-1}(t) = d_{-1}$ as a constant, one has

$$|\lambda_m| = 2v_{dc1} L_m (C'_1 + C'_2) d'_1. \quad (20)$$

Assume that $|\lambda_m|_{\max}$ is the maximum permissible flux linkage in the transformer for avoidance of the magnetic saturation, and then the constraint for the duty cycle change rate is given by

$$d'_1 < \frac{|\lambda_m|_{\max}}{2v_{dc1} L_m (C'_1 + C'_2)}. \quad (21)$$

- **MPPT With a Ramp-Changed Voltage Reference**

Usually speaking, L_m and $(C_1 + C_2)$ are relatively large because of the high permeability of the transformer core and the need energy storage capability of the dc-link capacitors to absorb the double-line-frequency power ripple. So, the constraint given by (21) can barely be satisfied if an MPPT method that produces a step-changed voltage reference is applied. In order to strictly follow (21), a customized MPPT method that periodically generates a ramp-changed voltage reference is developed in this paper.

- **Variable Step-Size MPPT Algorithm**

For simplicity, it is assumed that the PV module is working under the standard irradiance (1000 W/m²) and the room temperature (25 °C). Figure 8(a) sketches the operation curves of Sanyo HIT-210N, which best fits the proposed micro inverter. In Figure 8(b), d_{PPV}/dv_{PV} is illustrated. It is attraction mentioning that some MPPT techniques calculate the step size online relying on the instantaneous values of ΔPPV and Δv_{PV} in order to make the MPPT more adaptive [3], [36]. Though, the sensed ΔPPV and Δv_{PV} are susceptible to noises, chiefly, when they are small. Therefore, another method is adopted for robustness. Two points SPV1 and SPV2 on the d_{PPV}/dv_{PV} curve are selected to divide the PV operating points into three different zones, as shown in Figure 8(b). In zone 0, PV output power is close to the MPP, where a fine tracking step size is used to move toward the exact MPP. In zones 1 and 2, a larger tracking step size is applied to boost up the tracking speed. The adopted MPPT algorithm is shown in Figure 9. The tracking step sizes in zones 0, 1, and 2 are indicated by Δv_{ref0} , Δv_{ref1} , and Δv_{ref2} , respectively. k denotes the iteration number. In practice, Δv_{ref0} , Δv_{ref1} and Δv_{ref2} are selected as 0.1, 0.3, and 0.3V, correspondingly.

Screenshots PV Voltage & Current

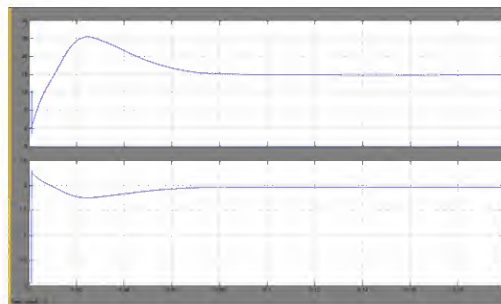


Figure 10

Grid Voltage & Current

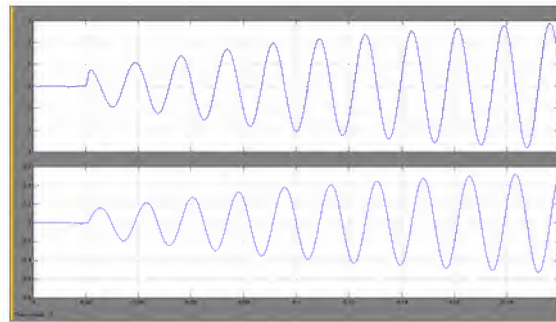


Figure 11

Capacitor Voltages

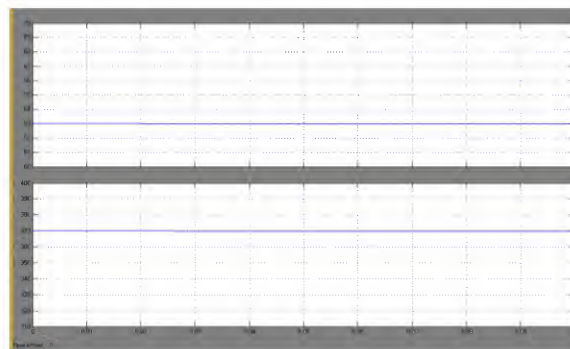


Figure 12

CONCLUSIONS

This paper presents a novel Repetitive Current control topology for grid-connected boost half- bridge photovoltaic (PV) micro inverter system. A plug-in repetitive current controller was presented and illustrated. The operation principles and dynamics of the boost-half-bridge dc–dc converter were examined and a customized MPPT control method was developed correspondingly. Here the minimal use of semiconductor devices, circuit simplicity, and easy control, the boost-half-bridge PV micro inverter possesses promising features of low cost and high reliability. According to the simulation results, high efficiency (97.0%–98.2%) is obtained with the boost-half-bridge dc–dc converter over a wide operation range. High power factor (>0.99) and low THD (0.9%–2.87%) are attained under both heavy load and light load conditions. Finally, the customized MPPT method that generates a ramp-changed reference for the PV voltage regulation which results a correct and reliable operation of the PV micro inverter system.

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